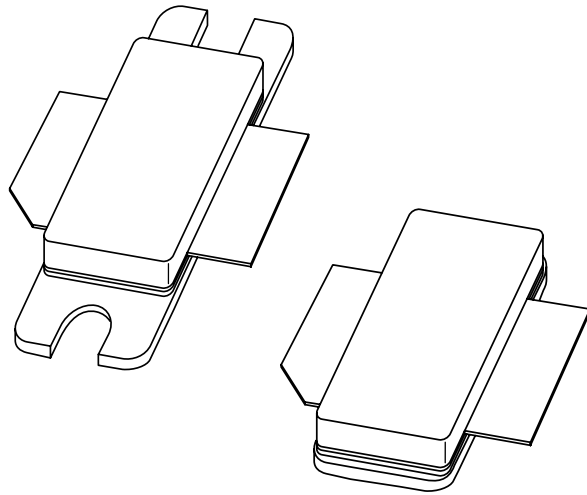


# DATA SHEET



## **BLF0810-90; BLF0810S-90** Base station LDMOS transistors

Preliminary specification

2002 Mar 18

Base station LDMOS transistors

BLF0810-90; BLF0810S-90

**FEATURES**

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (750 MHz to 1 GHz).

**APPLICATIONS**

- Common source class-AB operation in CDMA applications in the 750 to 960 MHz frequency range.

**DESCRIPTION**

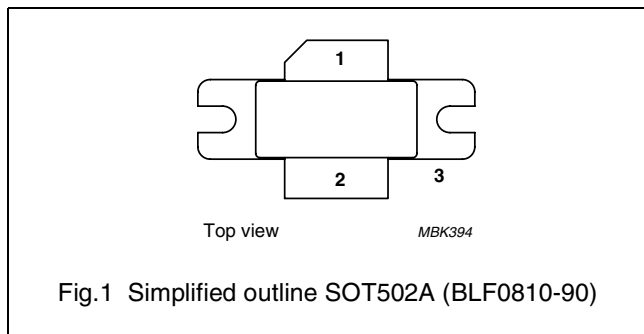
Silicon N-channel enhancement mode lateral D-MOS transistors encapsulated in a 2-lead flange package (BLF0810-90) with a ceramic cap or in a 2-lead earless package (BLF0810S-90). The common source is connected to the flange.

Typical CDMA IS95 performance at standard settings at a supply voltage of 27 V and  $I_{DQ} = 500$  mA

$P_L = 18$  W  
 $G_p = 16$  dB  
 $\eta = 26$  %  
 ACPR  $< -45$  dBc at 750 kHz and BW = 30 kHz  
 ACPR  $< -63$  dBc at 1.98 MHz and BW = 30 kHz

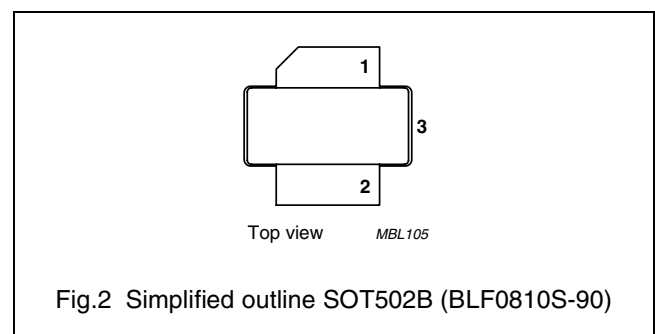
**PINNING - SOT502A**

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



**PINNING - SOT502B**

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



**QUICK REFERENCE DATA**

2-tone performance at  $T_h = 25$  °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ PEP (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_3$ (dBc)
Class-AB	881.4 - 881.6	27	60	typ. 16.5	typ. 35	typ. -30

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ avg (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR (dB)
CDMA <sup>(1)</sup>	881.5	27	18	typ. 16	typ. 26	typ. -46 <sup>(2)</sup> typ. -63 <sup>(3)</sup>

**Note**

1. IS95 CDMA (pilot, Paging, Sync, and Traffic Codes 8 trough 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz.

## Base station LDMOS transistors

## BLF0810-90; BLF0810S-90

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	75	V
$V_{GS}$	gate-source voltage		–	$\pm 15$	V
$T_{stg}$	storage temperature		–65	150	$^{\circ}\text{C}$
$T_j$	junction temperature		–	200	$^{\circ}\text{C}$

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	$T_h = 25\text{ }^{\circ}\text{C}$ , $P_L = 18\text{ W avg}$ , note 1	<0.75	K/W

**Note**

1. Thermal resistance is determined under RF operating conditions.

**CHARACTERISTICS**

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = 3\text{ mA}$	75	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 300\text{ mA}$	4	–	5	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = 36\text{ V}$	–	–	1	$\mu\text{A}$
$I_{DSX}$	on-state drain current	$V_{GS} = V_{GS(th)} + 9\text{ V}$ ; $V_{DS} = 10\text{ V}$	28	–	–	A
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\text{ V}$ ; $V_{DS} = 0$	–	–	1	$\mu\text{A}$
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ A}$	–	4.8	–	S
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 9\text{ V}$ ; $I_D = 10\text{ A}$	–	120	–	$\text{m}\Omega$

Base station LDMOS transistors

BLF0810-90; BLF0810S-90

APPLICATION INFORMATION

RF performance in a common source-AB circuit;  $T_h = 25\text{ }^\circ\text{C}$ .

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> PEP (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	d <sub>3</sub> (dBc)
Class-AB	881.4 - 881.6	27	500	60	>16	>35	<-30

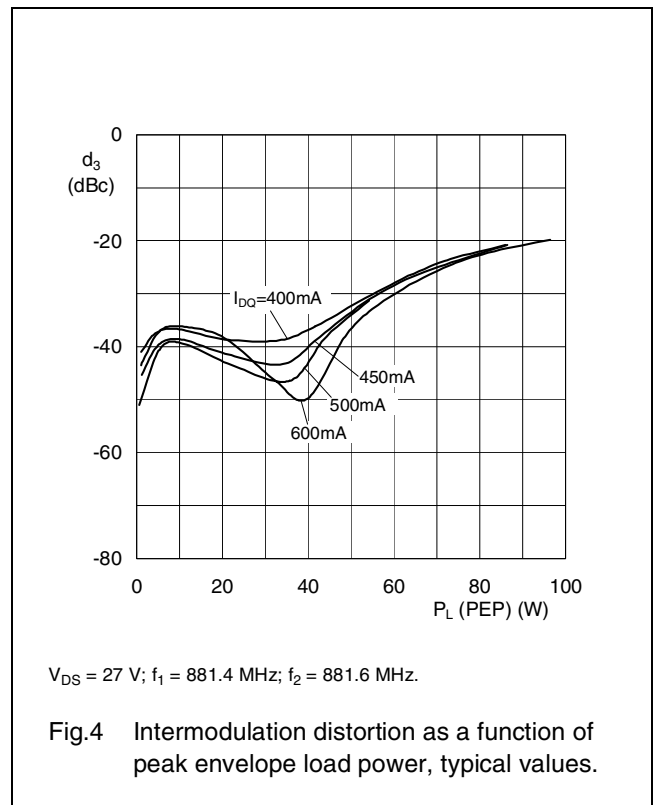
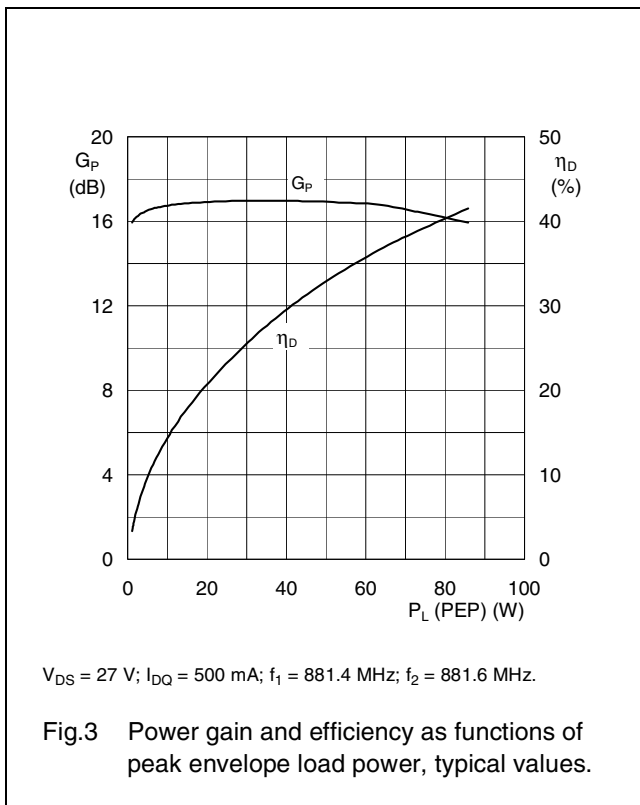
MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> avg (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	ACPR (dB)
CDMA <sup>(1)</sup>	881.5	27	500	>16	>15	>26	<-46 <sup>(2)</sup> <-63 <sup>(3)</sup>

Note

- IS95 CDMA (pilot, Paging, Sync, and Traffic Codes 8 trough 13)
- ACPR 750 kHz at BW = 30 kHz
- ACPR 1.98 MHz at BW = 30 kHz.

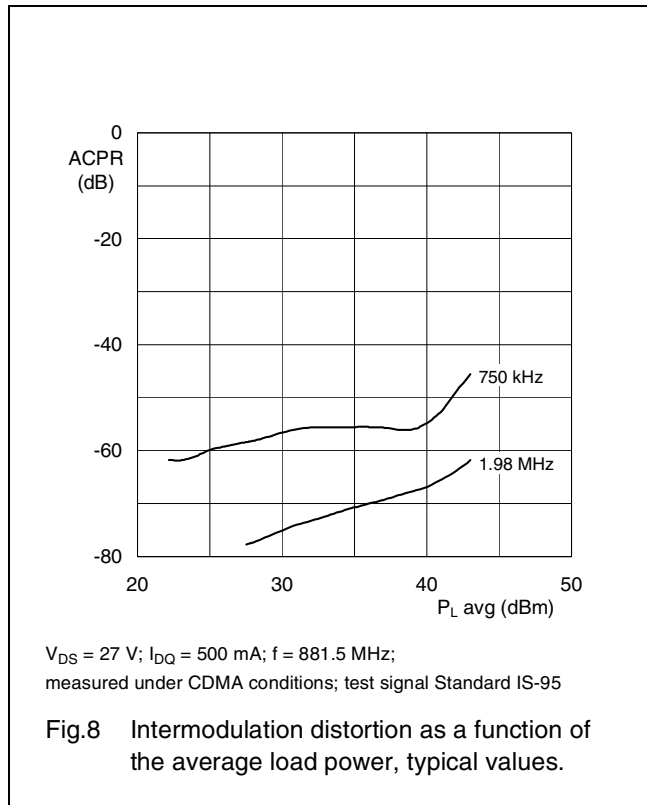
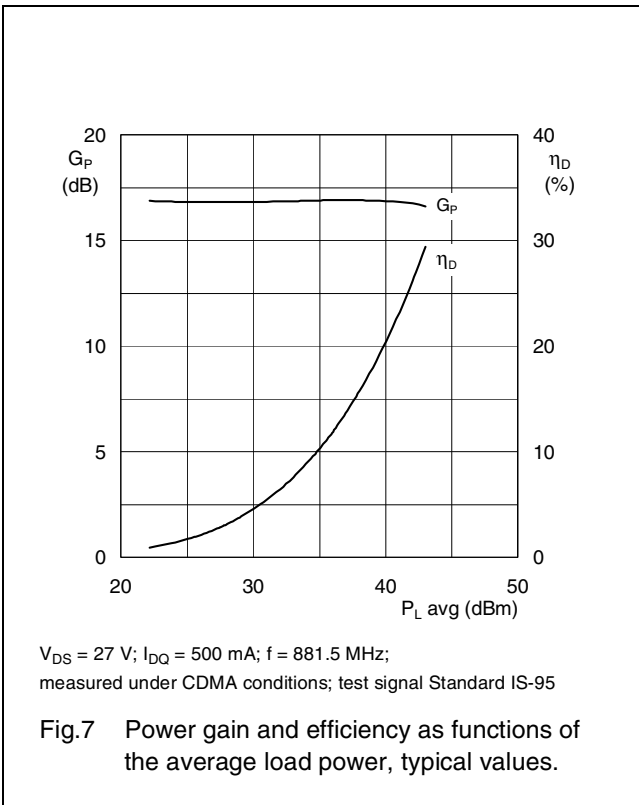
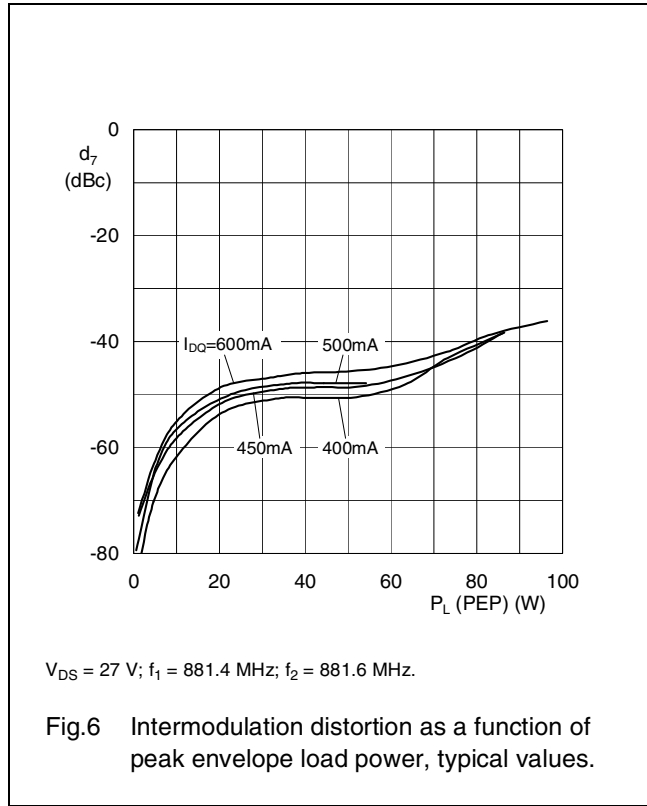
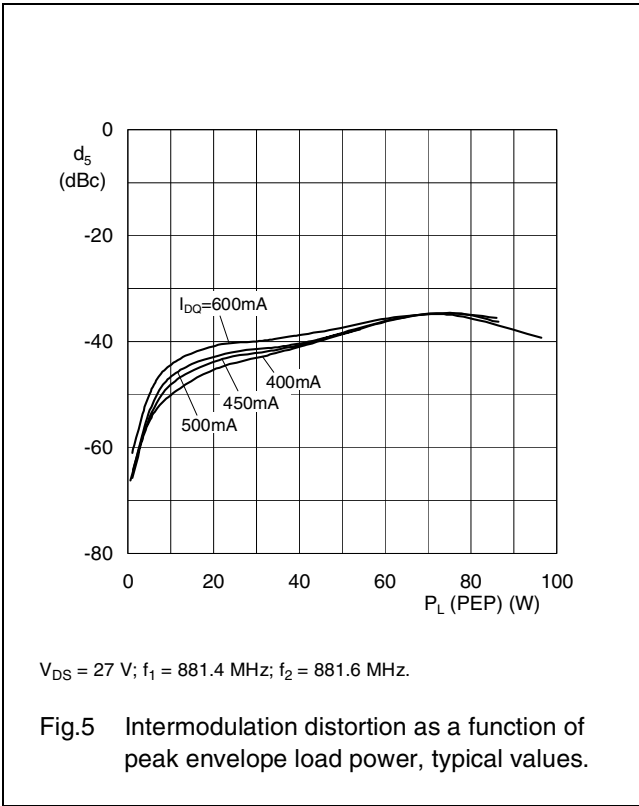
Ruggedness in class-AB operation

The BLF0810-90 and BLF0810S-90 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases at V<sub>DS</sub> = 27 V; P<sub>L</sub> = 60 W (PEP).



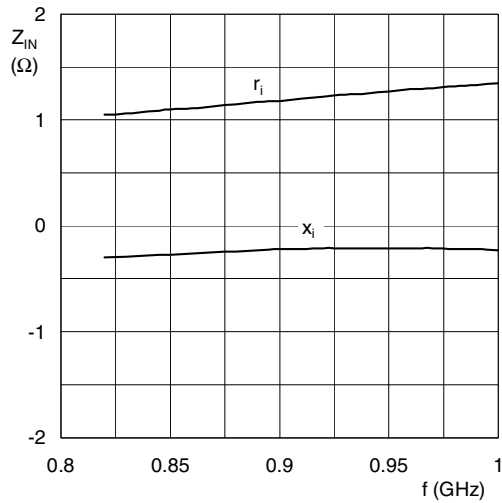
Base station LDMOS transistors

BLF0810-90; BLF0810S-90



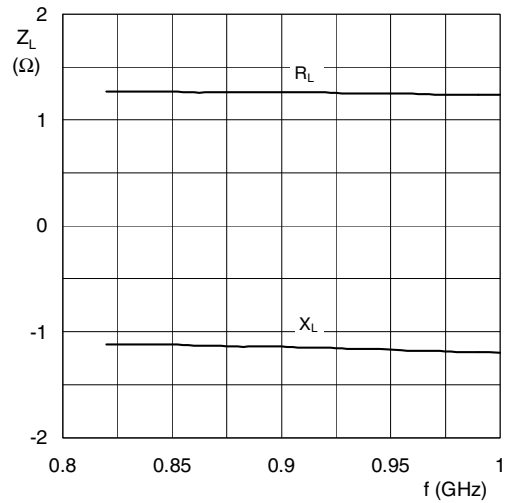
Base station LDMOS transistors

BLF0810-90; BLF0810S-90



Class-AB operation;  $V_{DS} = 27$  V;  $I_{DQ} = 500$  mA;  $P_L = 18$  W.

Fig.9 Input impedance as a function of frequency (series components); typical values.



Class-AB operation;  $V_{DS} = 27$  V;  $I_{DQ} = 500$  mA;  $P_L = 18$  W.

Fig.10 Load impedance as a function of frequency (series components); typical values.

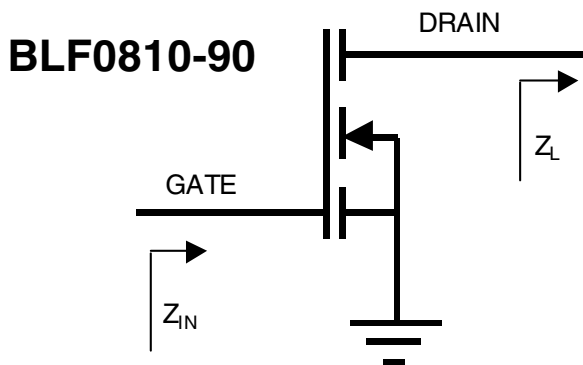


Fig.11 Definition of transistor impedance.

Base station LDMOS transistors

BLF0810-90; BLF0810S-90

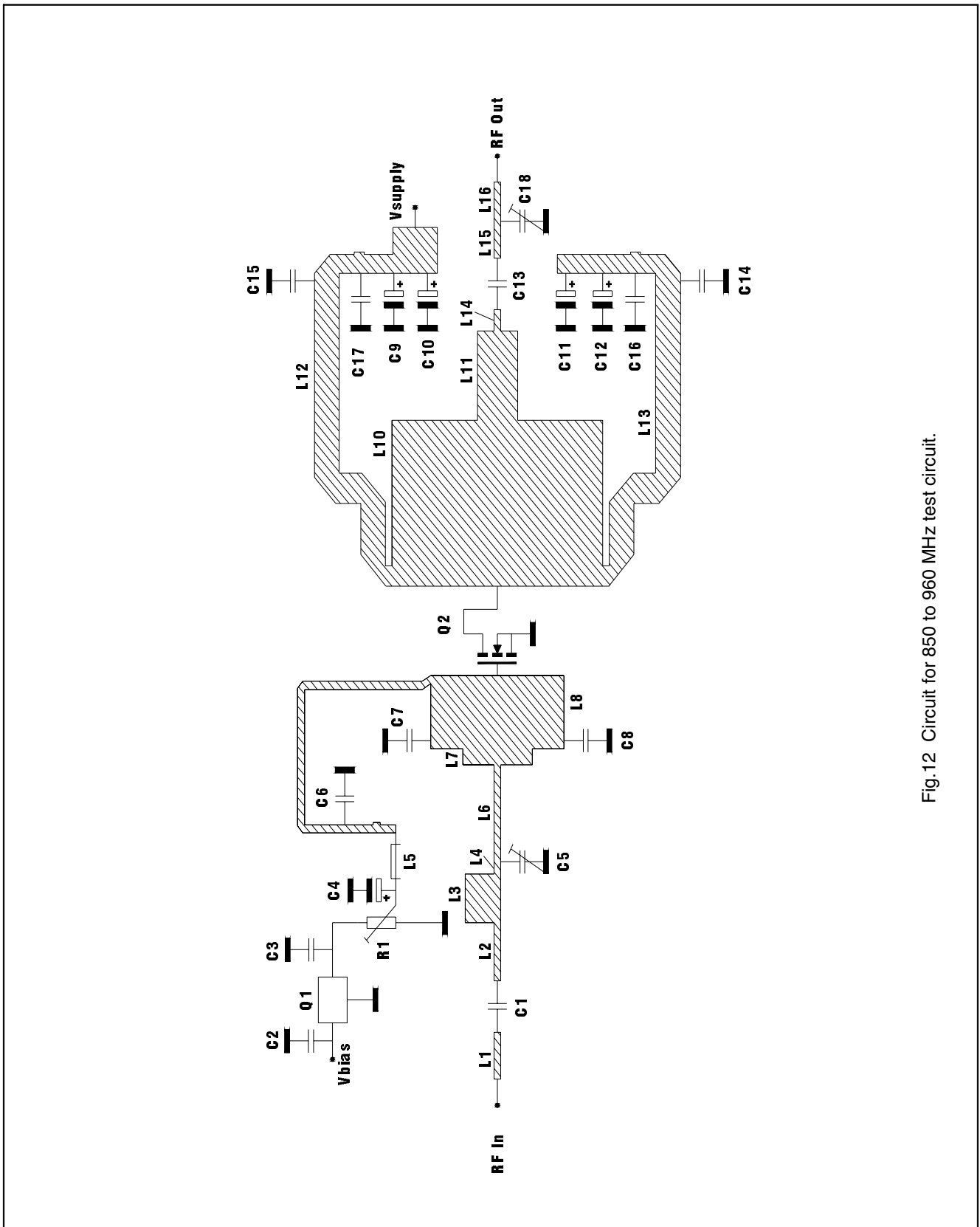


Fig.12 Circuit for 850 to 960 MHz test circuit.

Base station LDMOS transistors

BLF0810-90; BLF0810S-90

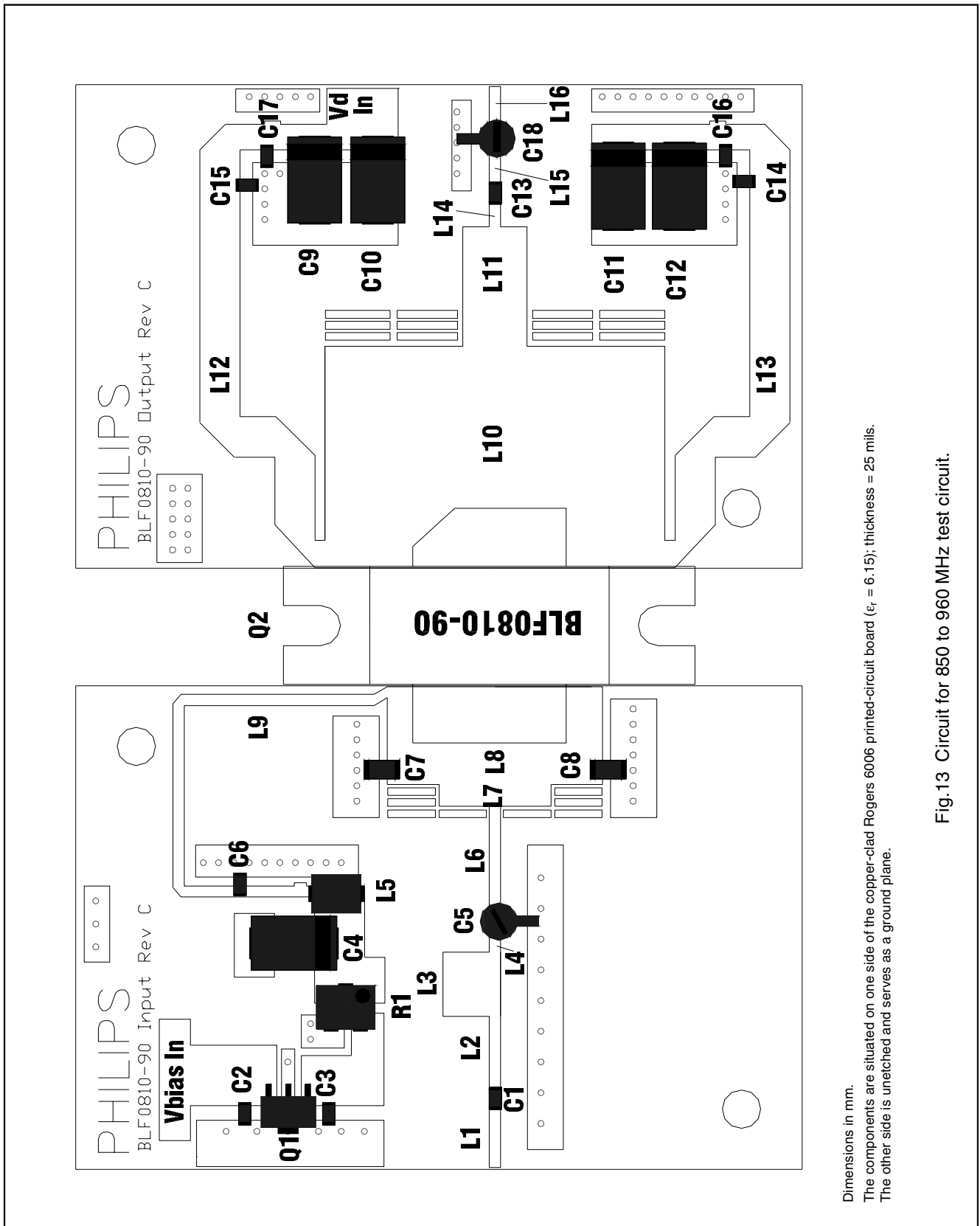


Fig.13 Circuit for 850 to 960 MHz test circuit.

Dimensions in mm.  
The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board ( $\epsilon_r = 6.15$ ); thickness = 25 mils.  
The other side is unetched and serves as a ground plane.



## Base station LDMOS transistors

## BLF0810-90; BLF0810S-90

## List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 $\mu$ F	
C5, C18	air trimmer capacitor	8 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 k $\Omega$	
Q1	7808 voltage regulator		
Q2	BLF0910-140 LDMOS transistor		
L1	stripline; note 2		204 $\times$ 36 mils
L2	stripline; note 2		253 $\times$ 36 mils
L3	stripline; note 2		210 $\times$ 188 mils
L4	stripline; note 2		94 $\times$ 36 mils
L5	Ferroxcube		
L6	stripline; note 2		380 $\times$ 36 mils
L7	stripline; note 2		71 $\times$ 363 mils
L8	stripline; note 2		319 $\times$ 700 mils
L9	stripline; note 2		1724 $\times$ 36 mils
L10	stripline; note 2		721 $\times$ 1106 mils
L11	stripline; note 2		389 $\times$ 210 mils
L12, L13	stripline; note 2		1470 $\times$ 131 mils
L14	stripline; note 2		92 $\times$ 36 mils
L15, L16	stripline; note 2		165 $\times$ 36 mils

## Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ( $\epsilon_r = 6.15$ ); thickness = 25 mils.

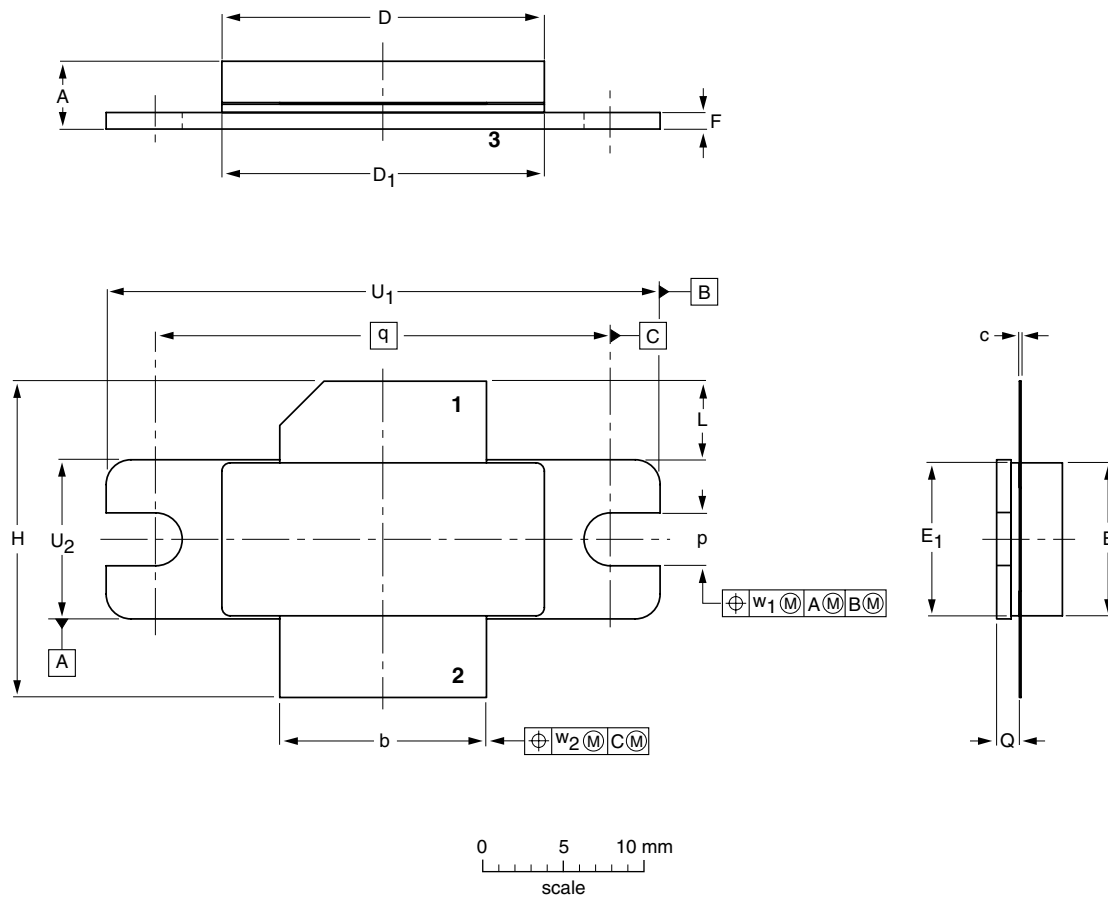
Base station LDMOS transistors

BLF0810-90; BLF0810S-90

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						<del>99-10-13</del> 99-12-28

Base station LDMOS transistors

BLF0810-90; BLF0810S-90

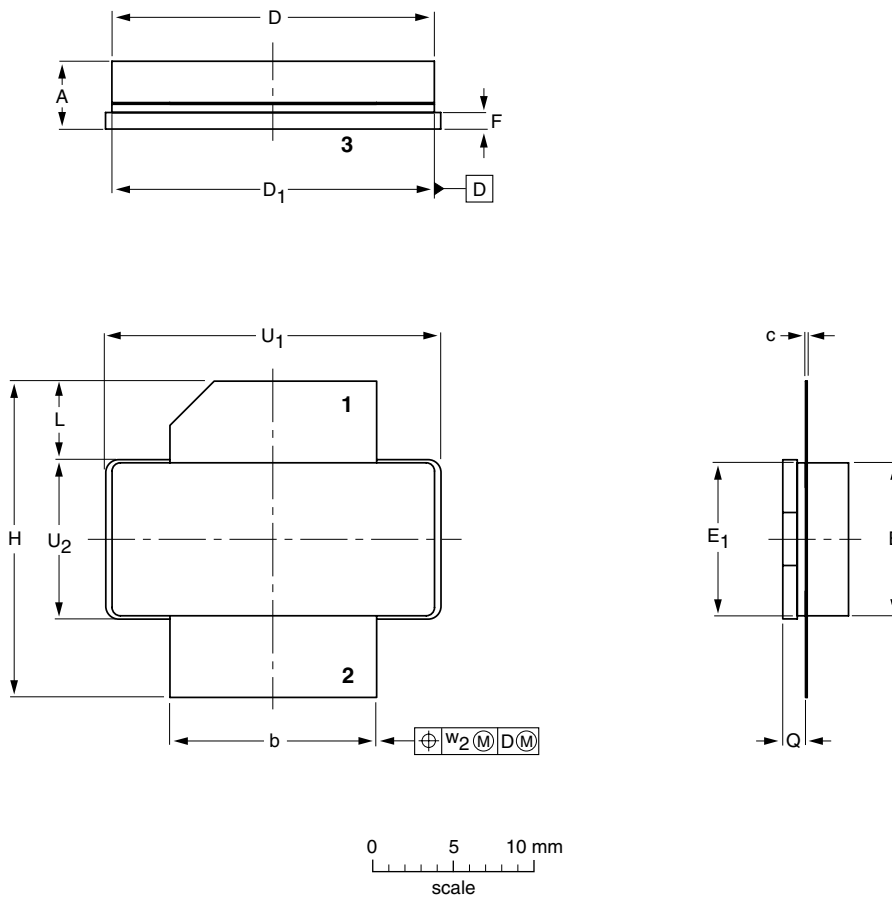
PACKAGE OUTLINE

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

**Package under development**

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	Q	U <sub>1</sub>	U <sub>2</sub>	w <sub>2</sub>
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502B						99-12-16 99-12-28

## Base station LDMOS transistors

## BLF0810-90; BLF0810S-90

## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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